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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,393	03/26/2001	Funitomo Matsuoka	205173US2S	7222

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TOLEDO, FERNANDO L

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2823

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/816,393	MATSUOKA, FUNITOMO
	Examiner Fernando Toledo	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 31 July 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 14-18 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-13 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 26 March 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

1. Claims 14 – 18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.
2. Applicant's election without traverse of claims 1 – 13 in Paper No. 5 is acknowledged.

Information Disclosure Statement

3. The information disclosure statement filed 3/26/01 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because it lacks an English translation either of the abstract or the whole document of the foreign reference. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Drawings

4. Figures 1 – 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. *The objection to the drawings will not be held in abeyance.*

Specification

5. The disclosure is objected to because of the following informalities: Throughout the specification the list shortening abbreviation "etc." is used inappropriately since there is no list to shorten. Example of such can be found on page 4 of the specification in line 17.

Appropriate correction is required.

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Yu (U. S. patent 6,225,173 B1).

In re claim 1, AAPA discloses forming a dummy gate electrode on a semiconductor substrate (figure 1); with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in those regions of the semiconductor substrate which are opposite to each other through the dummy gate electrode (figure 1);

forming an insulating film on the semiconductor substrate in a way to bury the dummy gate electrode, while exposing an upper surface of the gate electrode (figure 4); removing the dummy gate electrode and forming a first trench in the insulating film (figure 4); forming a gate insulating film along the inner surface of the second trench (figure 7); forming a gate electrode in the second trench with the gate insulating film intervening therebetween (figure 8).

AAPA does not show, enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench.

However, Yu, in the U. S. patent 6,225,173 B1; figures 1 – 5 and related text, disclose enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench (figures 4 and 5) to form an ultra-shallow source extension and an ultra-shallow drain extension (column 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to enlarge the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench, in the AAPA invention, because, as taught by Yu, it forms an ultra-shallow source extension and an ultra-shallow drain extension.

In re claim 2, AAPA discloses after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall surface of the dummy gate electrode (figure 2); and with the dummy gate electrode and the side wall insulating film used as a

mask, forming second impurity diffusion region layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers (figure 2).

In re claim 3, Yu discloses wherein the step of forming a second trench includes a step of performing an isotropic etching on the insulating film having the first trench formed therein (column 4).

In re claim 4, AAPA discloses the step of forming a gate insulating film includes a step of forming a gate insulating film in a manner to make the width of the second trench equal to, or greater than, that of the first trench (page 5).

In re claim 5, AAPA discloses wherein the step of forming the gate insulating layer includes a step of using an insulating material having a relative dielectric constant of above 5 (page 5).

In re claim 6, AAPA discloses wherein the step of forming a gate insulating film includes a step of using one selected from the group consisting of Ta₂O₅, silicon nitride, Al₂O₃, BaSrTiO₃, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

In re claim 7, AAPA discloses forming a first insulating film on a semiconductor substrate (figure 1); sequentially forming a first semiconductor film and a second insulating film on the first insulating film (figure 1); forming a resist pattern on the second insulating film (figure 1); with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate (figure 1); with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity

diffusion layers for a source and a drain (figure 1); forming a third insulating film over the semiconductor structure to bury the stacked layer structure (figure 4); etching back the third film to expose an upper surface of the stacked layer structure (figure 4); with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film (figure 4); depositing a fourth insulating film along an inner surface of the trench (figure 7); forming a conductive layer of a gate electrode on the fourth insulating film (figure 8).

AAPA does not show, enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench.

However, Yu, in the U. S. patent 6,225,173 B1; figures 1 – 5 and related text, disclose enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench (figures 4 and 5) to form an ultra-shallow source extension and an ultra-shallow drain extension (column 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to enlarge the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench, in the AAPA invention, because, as taught by Yu, it forms an ultra-shallow source extension and an ultra-shallow drain extension.

In re claim 8, AAPA discloses after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer structure (figure 2); with the sidewall insulating film and the stacked layer structure used as a mask, forming

second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first diffusion layers (figure 2).

In re claim 9, AAPA in view of Yu does not teach wherein the step of enlarging the width of the trench includes a step of using, as the isotropic etching, an etching treatment including HF and NH₄F.

However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to use in the isotropic etching to enlarge the width of the trench an etching treatment including HF and NH₄F since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

In re claim 10, AAPA discloses depositing a fourth insulating film by a CVD or a sputtering method (page 5).

In re claim 11, AAPA discloses wherein the step of depositing a fourth insulating film includes a step of forming the fourth insulating film to make the width of the trench after forming the fourth insulating film equal to, or greater than, that of the first trench (page 6).

In re claim 12, AAPA discloses wherein the step of forming the gate insulating layer includes a step of using an insulating material having a relative dielectric constant of above 5 (page 5).

In re claim 13, AAPA discloses wherein the step of forming a gate insulating film includes a step of using one selected from the group consisting of Ta₂O₅, silicon nitride, Al₂O₃, BaSrTiO₃, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

Conclusion

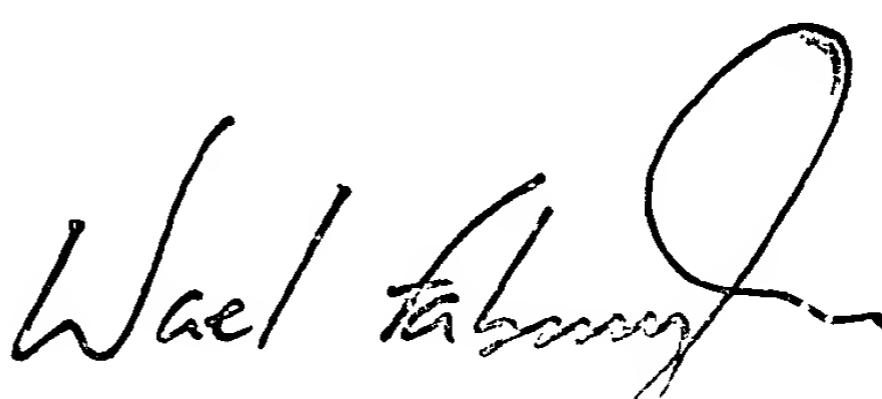
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is 703-305-0567. The examiner can normally be reached on Mon-Fri 8am to 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Fernando Toledo
Examiner
Art Unit 2823

ft
August 21, 2002



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